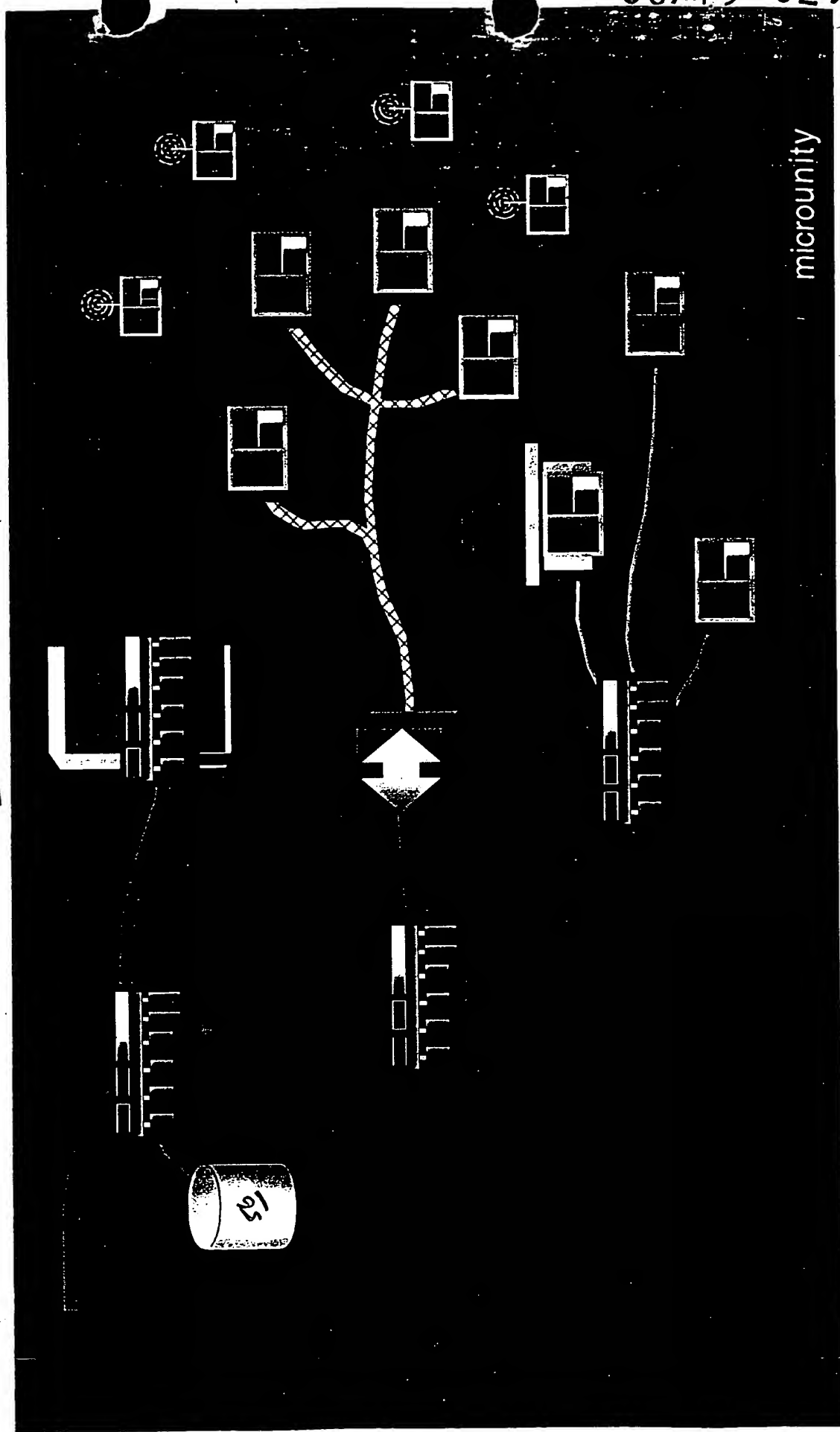


Figure 1

microunity

Figure 2



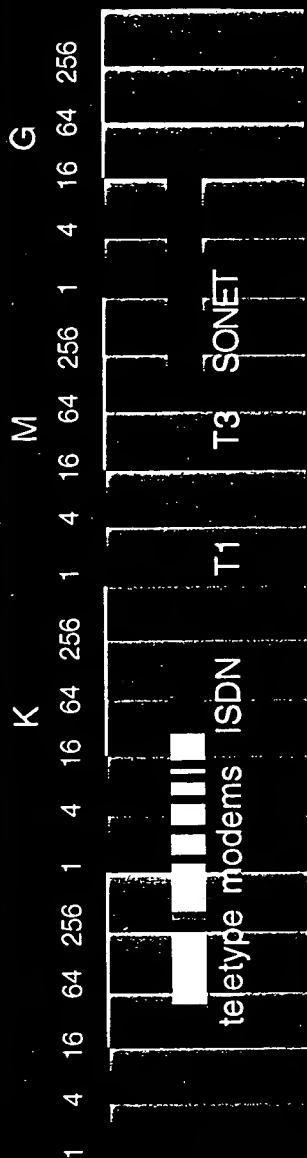
2001-2002-2003-2004-2005

31

Figure 3

(BITS / SECOND)

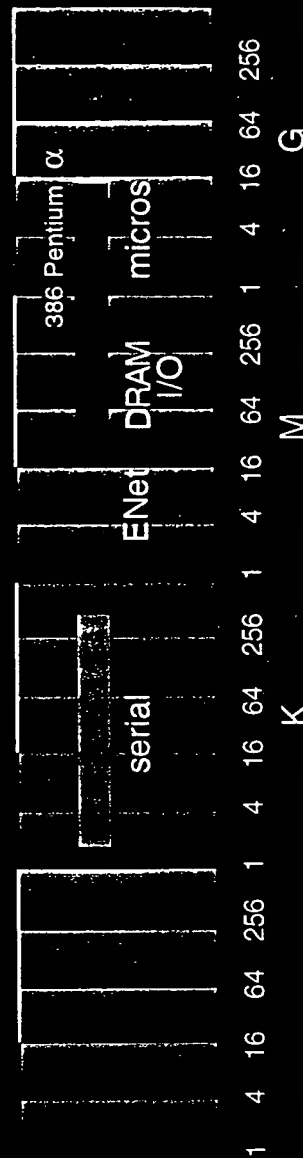
Telecom



Media



Computing

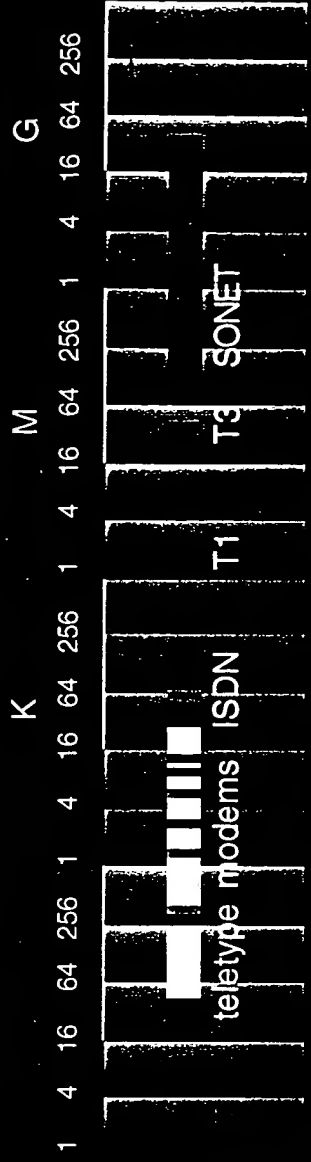


microunity

Figure 4

(BITS / SECOND)

Telecom



Media

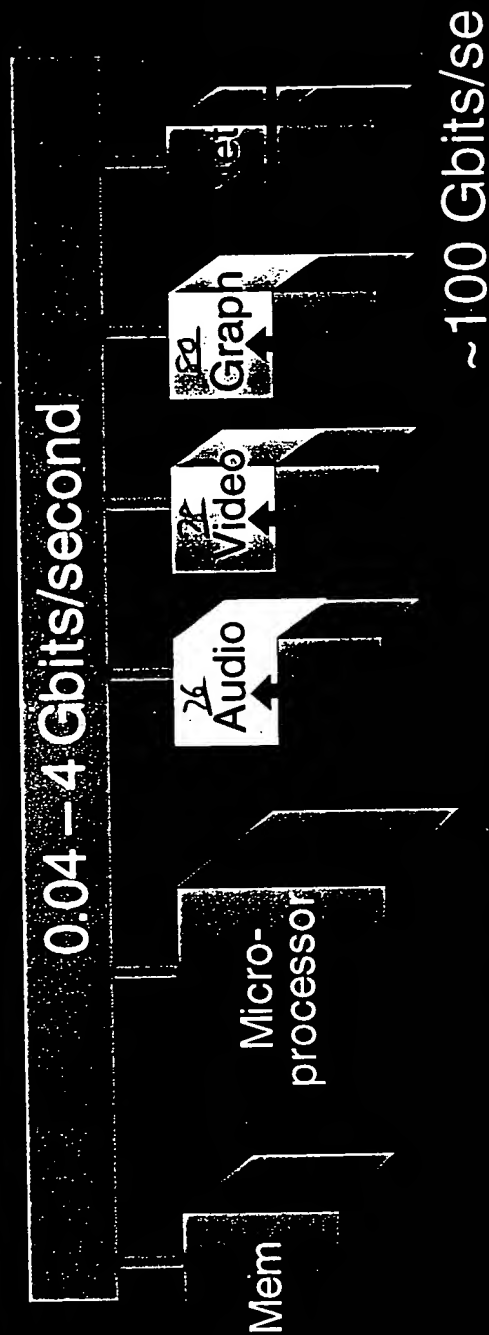


Computing



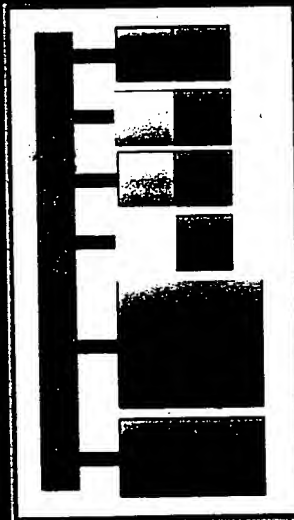
microunity

Figure 5



~100 Gbits/se

The Future of the Old Way (1999)

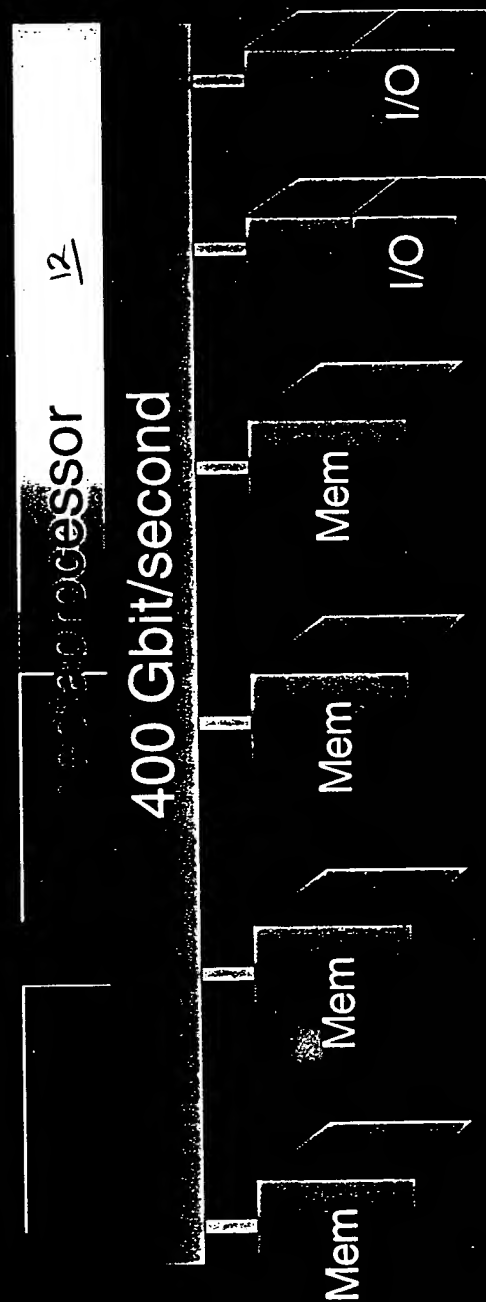


- single chip
- lower cost

Mem

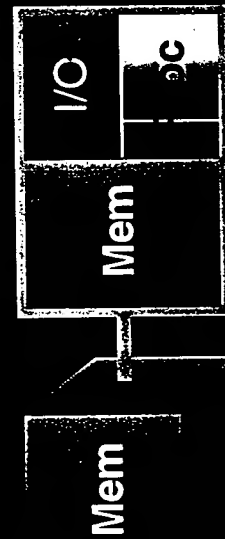
microunity

Figure 6



The Future of the Unified Way (1995)

- smaller chip
- much lower cost



2004-02-25-230

Figure 7

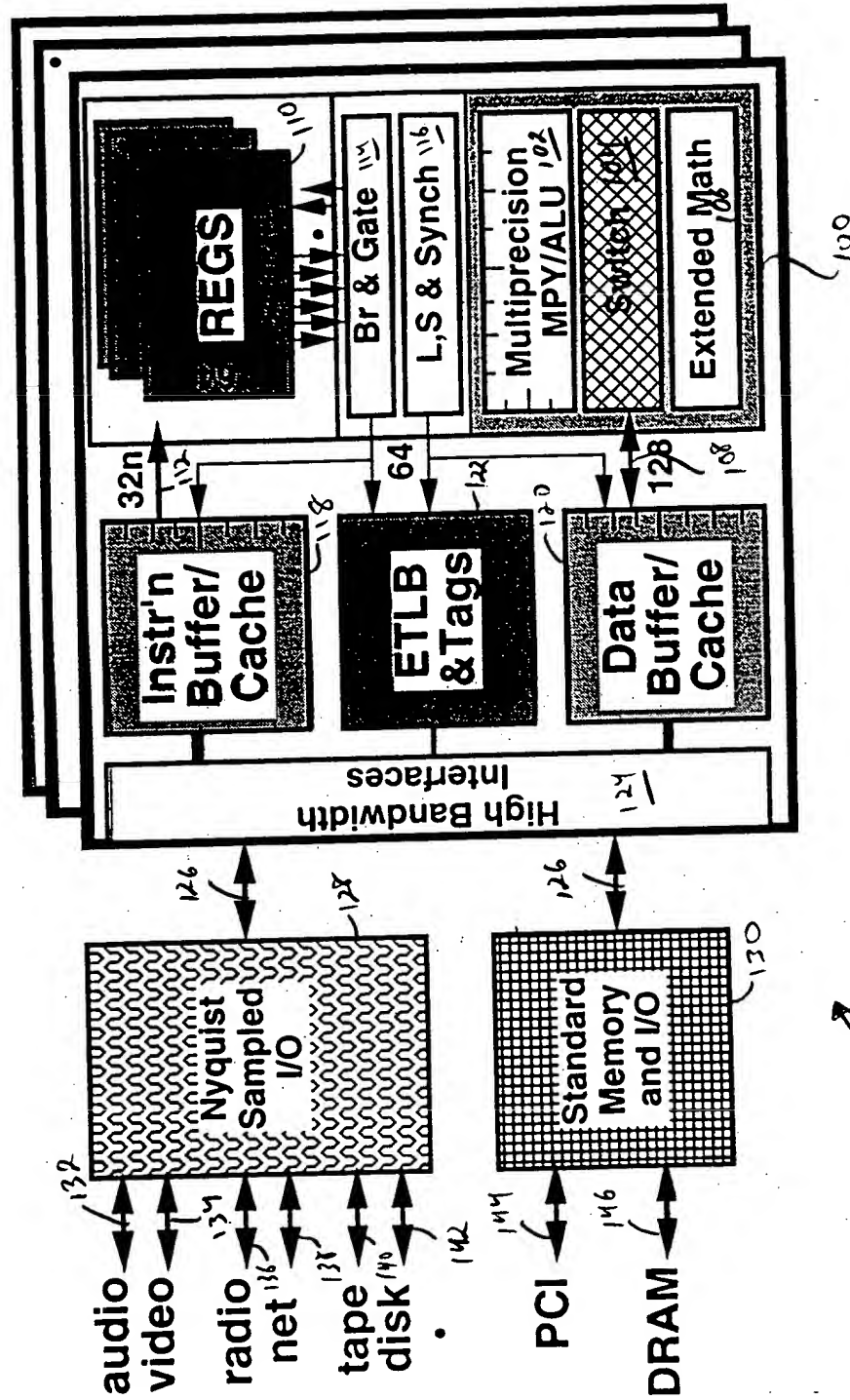


Figure 8(a)

Group Expand

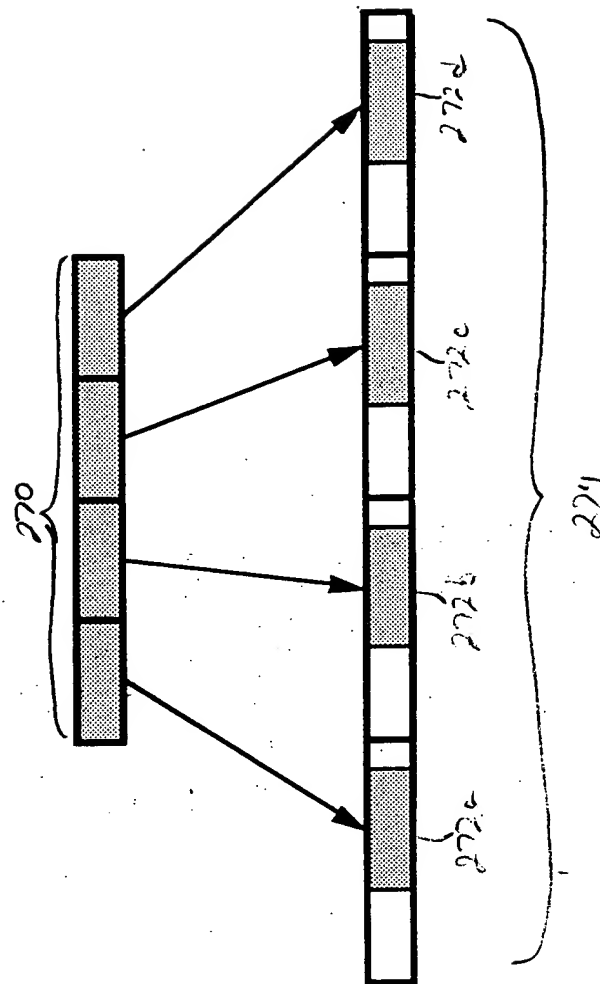


Figure 8(b)
Group Compress, Extract

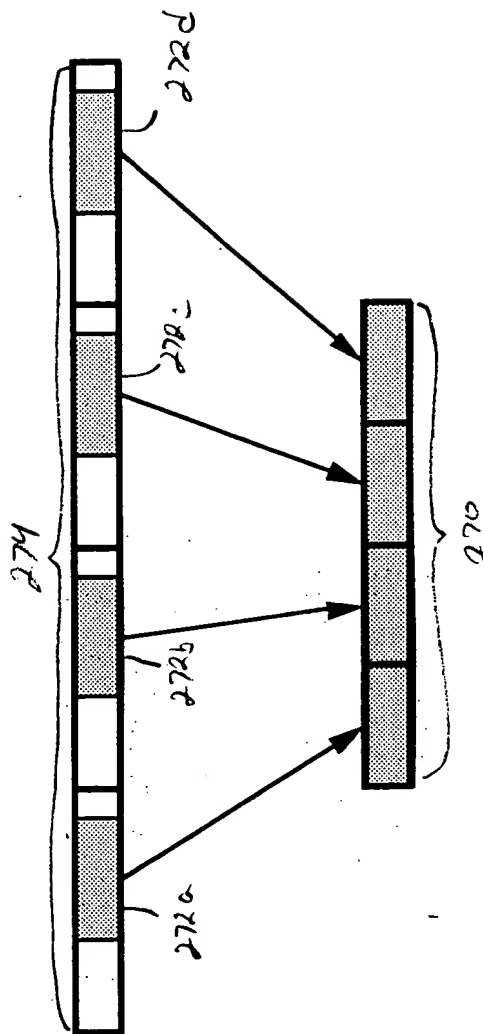
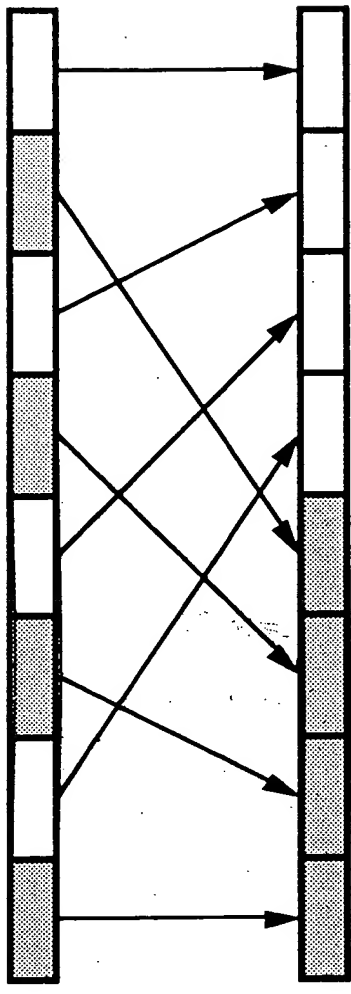


Figure 8(c)

Group Deal, Shuffle

- Group Deal: 128 bits to 128 bits



- Group Shuffle: 128 bits to 128 bits

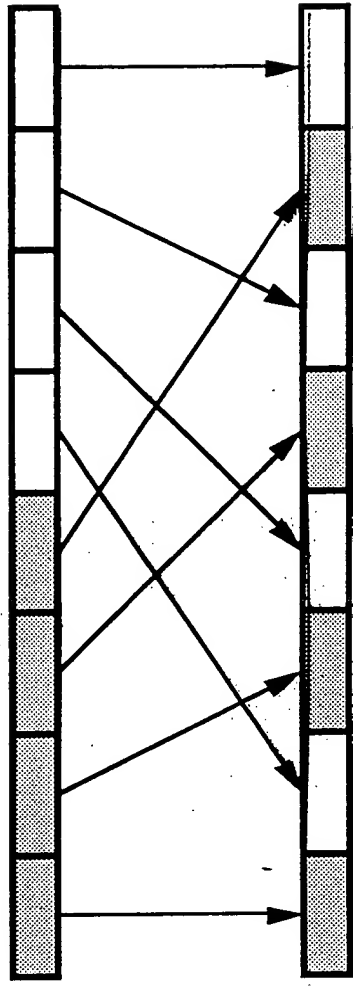


Figure 8(d)

Group Swizzle (Copy-Swap)

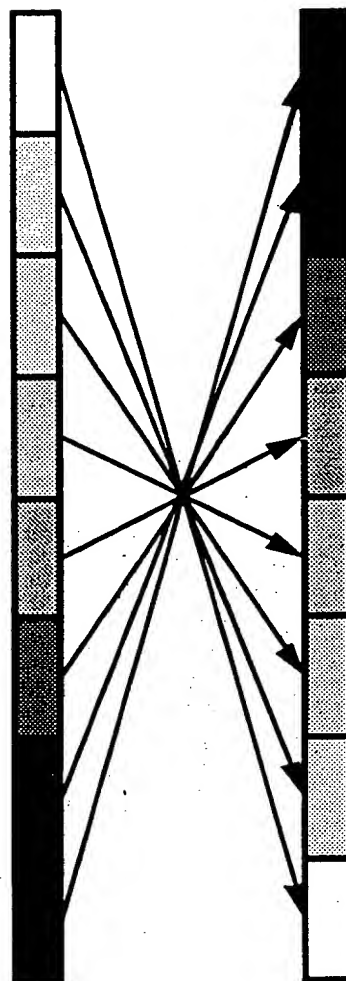


Figure 8(e)

Group Permute

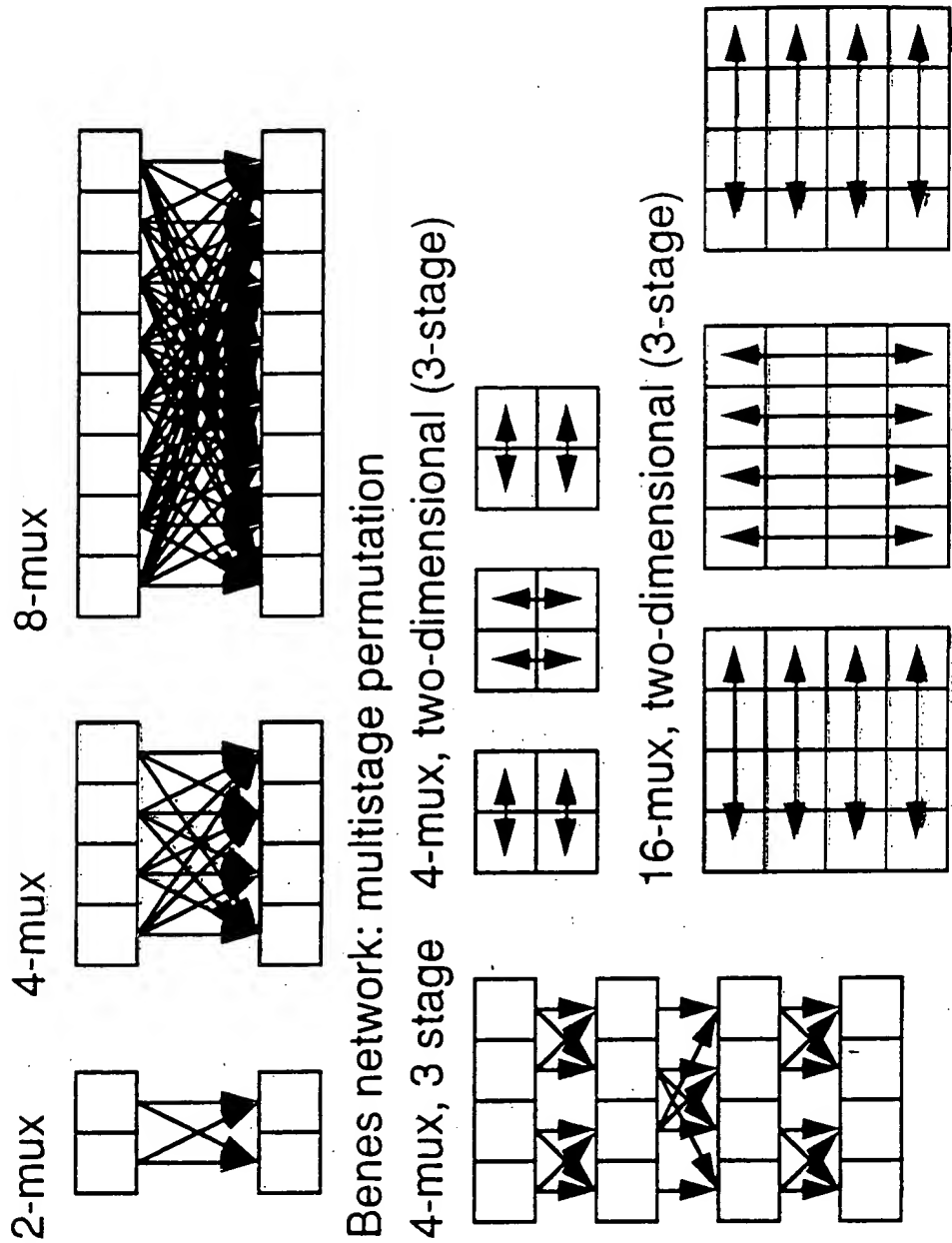


Figure 9(a)

Instruction Formats

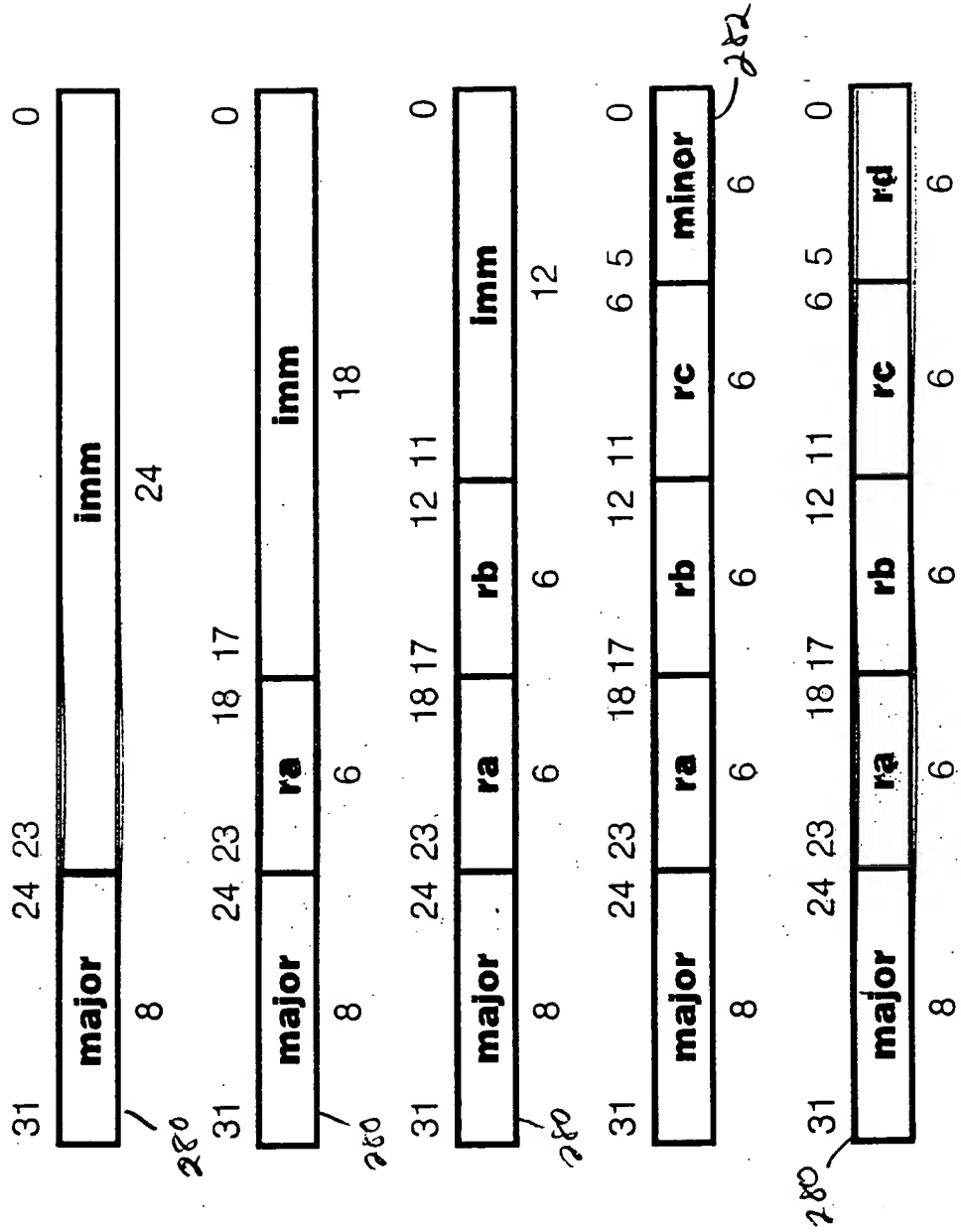


Figure 9(b)

Floating-point Data Sizes

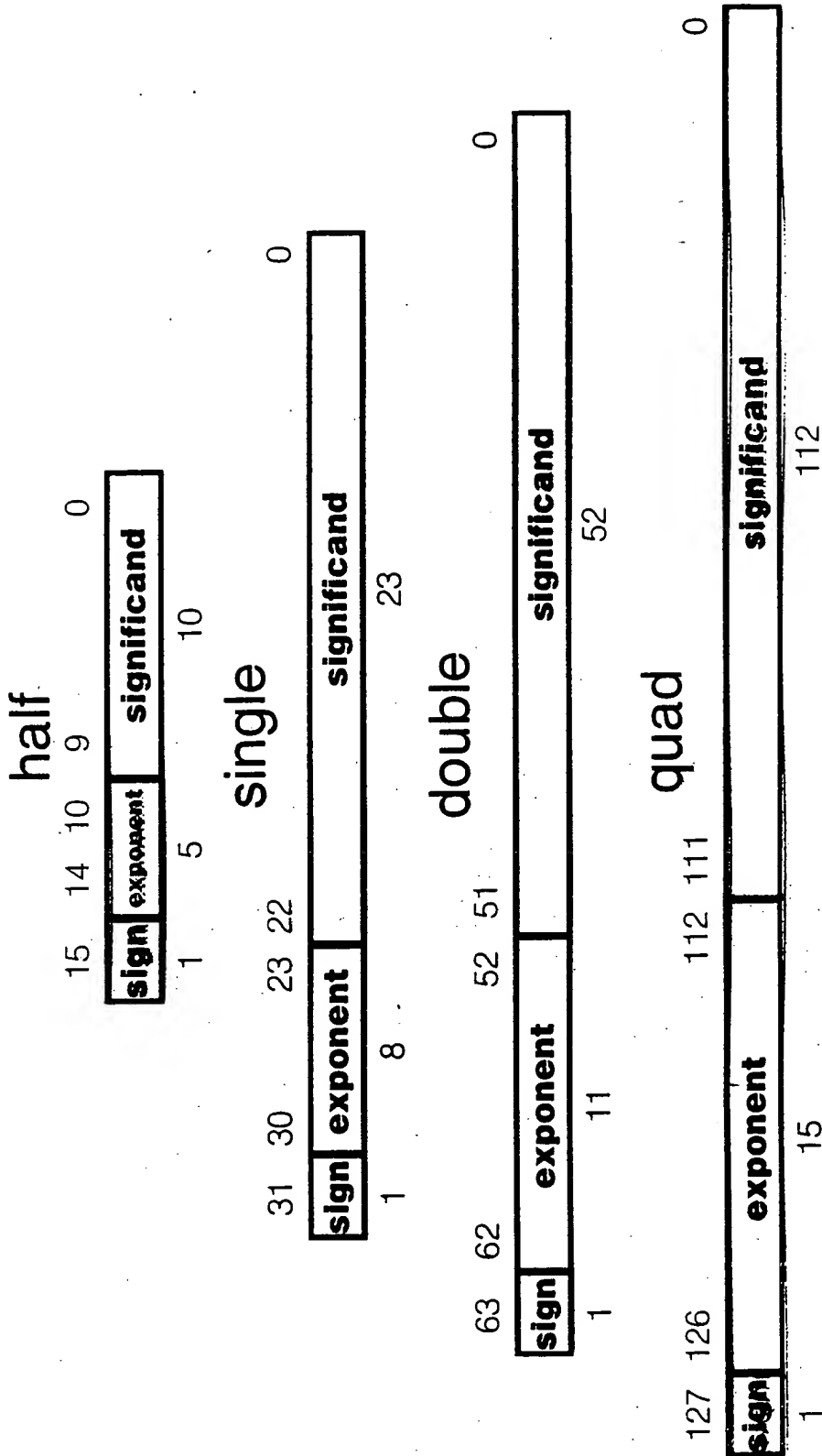


Figure 9(c)

Fixed-Point Data Sizes

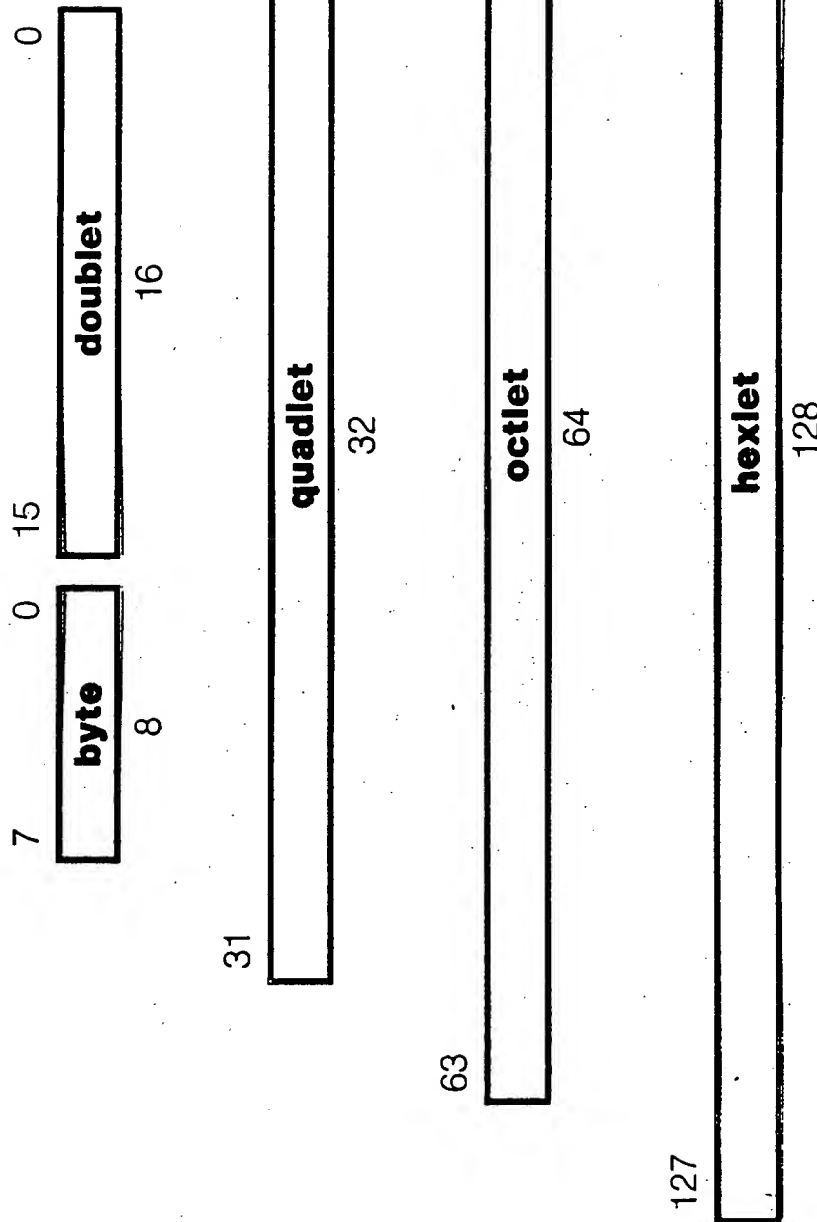


Figure 10(a)

Translation Block Diagram

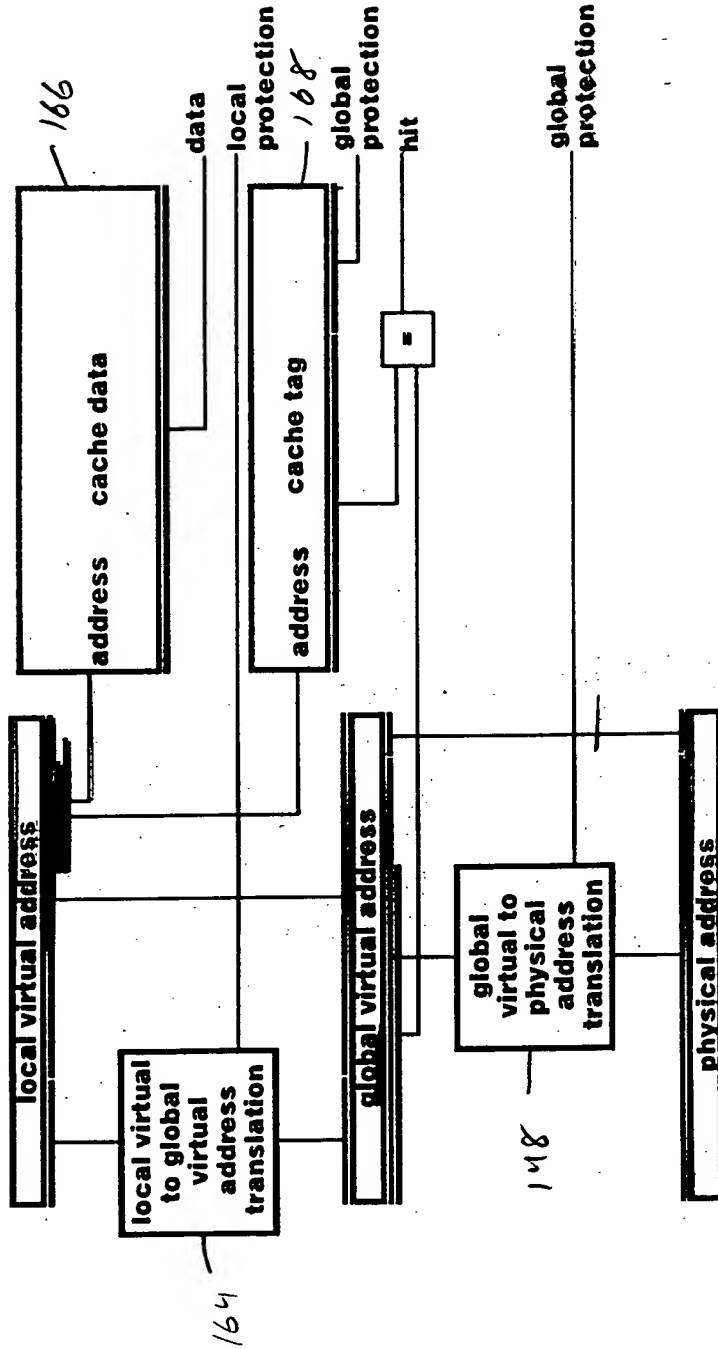


Figure 10(b)

Translation Lookaside Buffer

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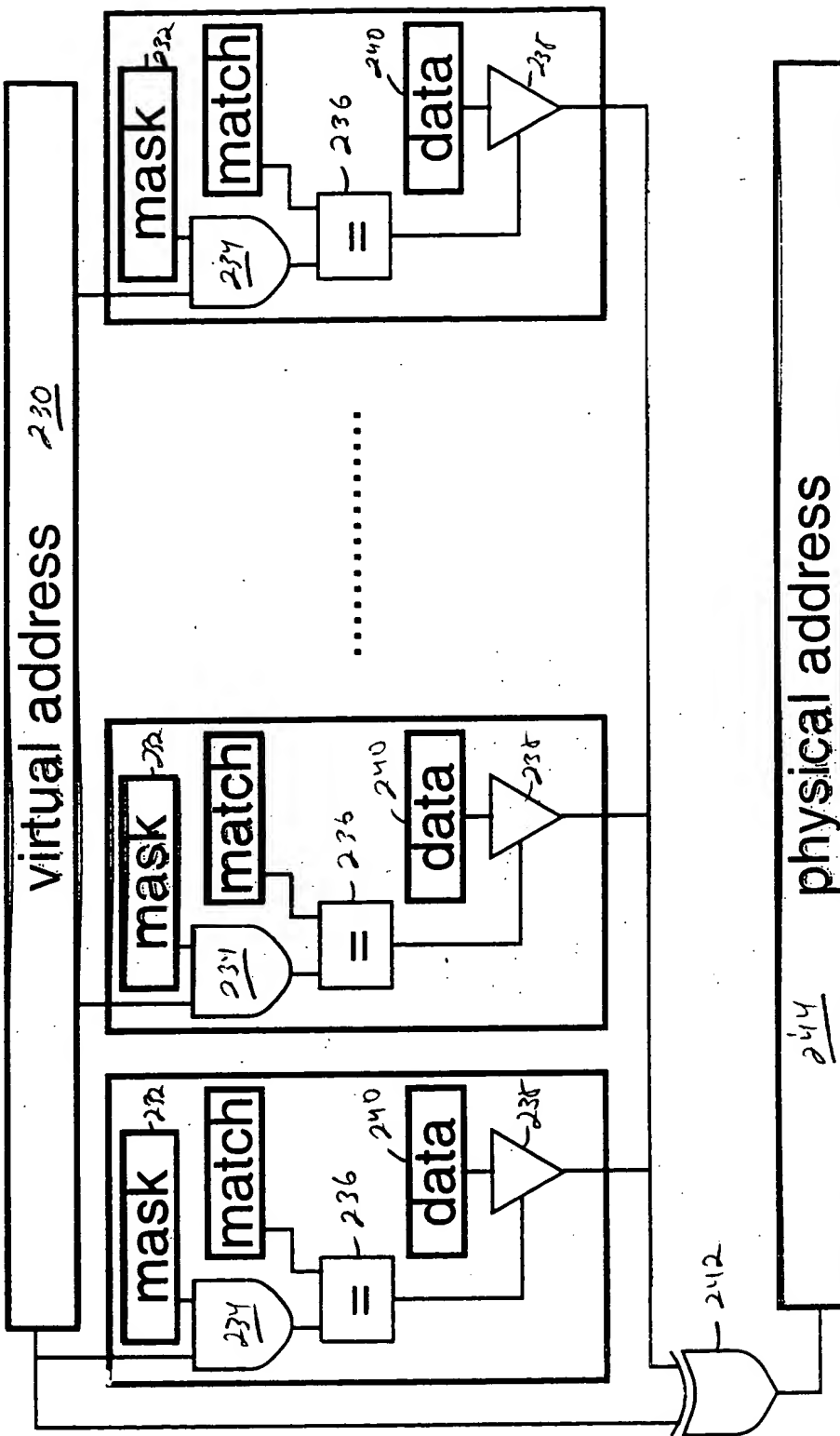


Figure 11

Superstring Pipeline

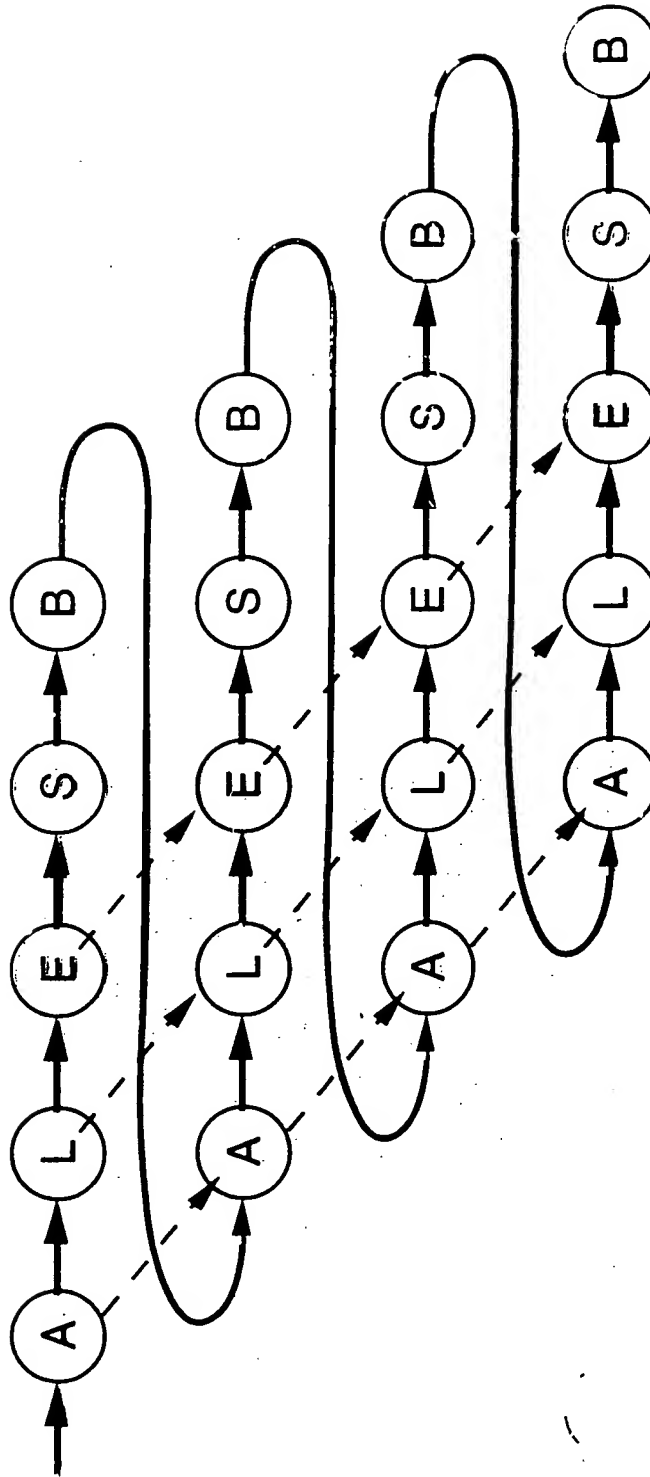


Figure 12

Superspring Pipeline

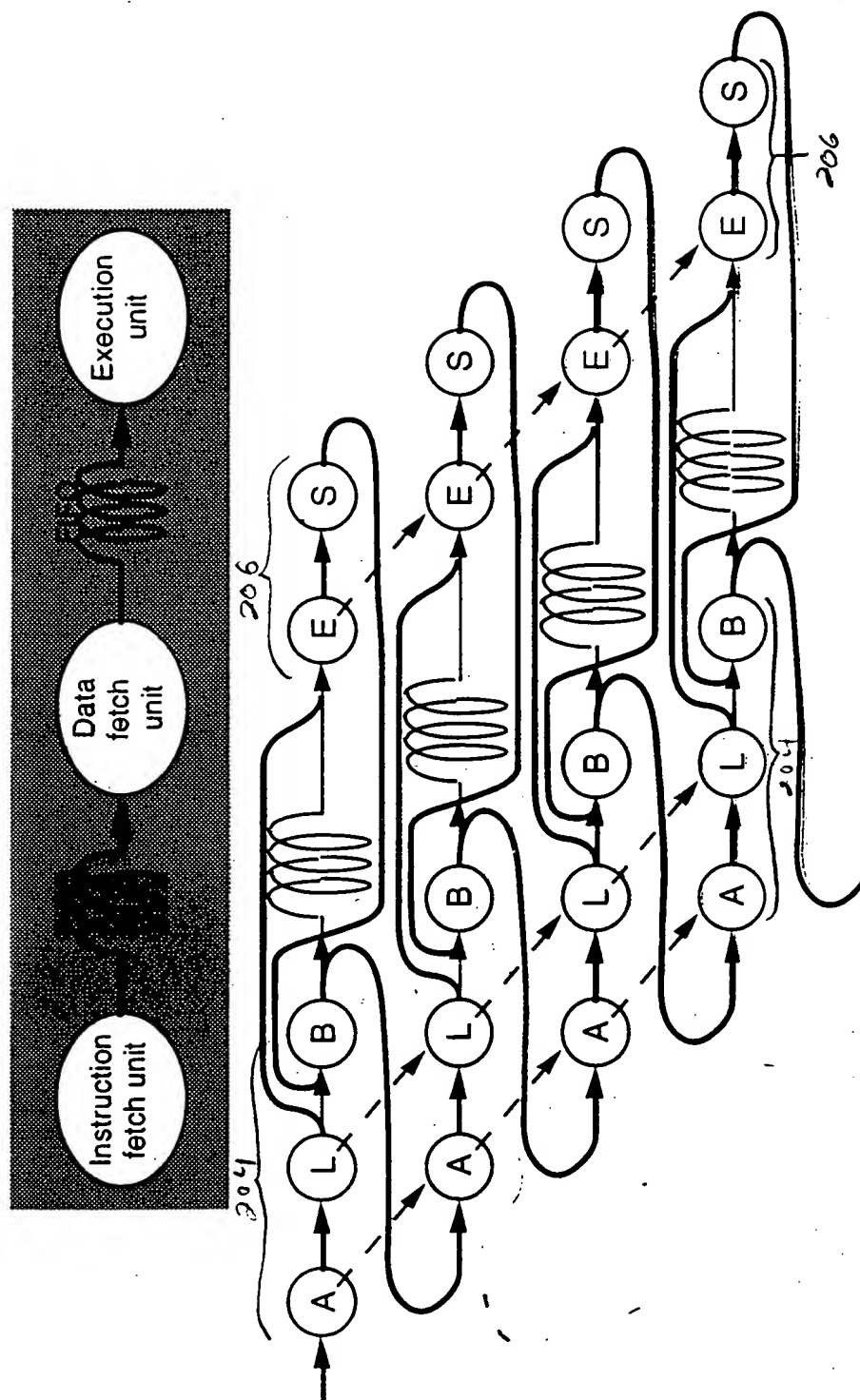
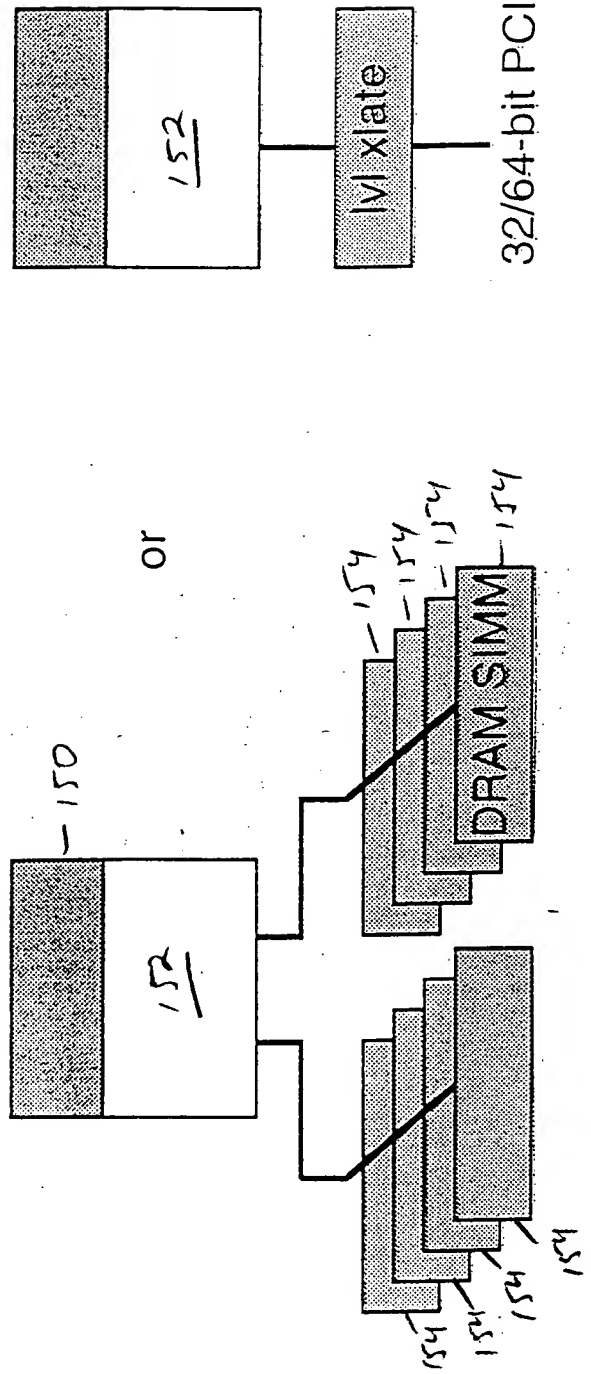


Figure 1 is a block diagram of a multi-processor system. It shows four identical processing units, each labeled 150. Each unit contains a 64 KByte Cache (156a) and a DRAM CTL (156b). The caches are connected to a common 72-bit data bus (160). Each unit also has its own 72-bit data bus (162) connected to DRAMs (154). A 16-bit address bus (164) and a 4-bit control bus (166) are shown at the bottom.

2007-08-20

Figure 14



L66120-02B15.130

Figure 15

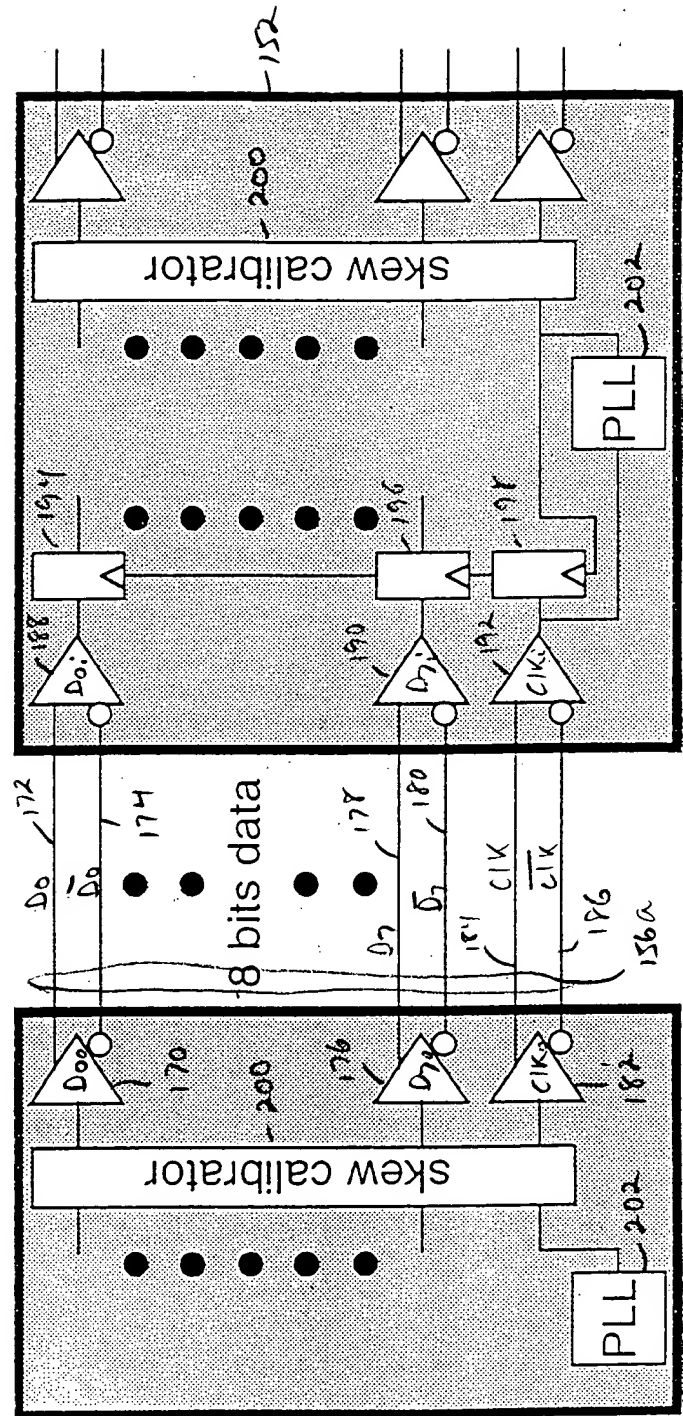
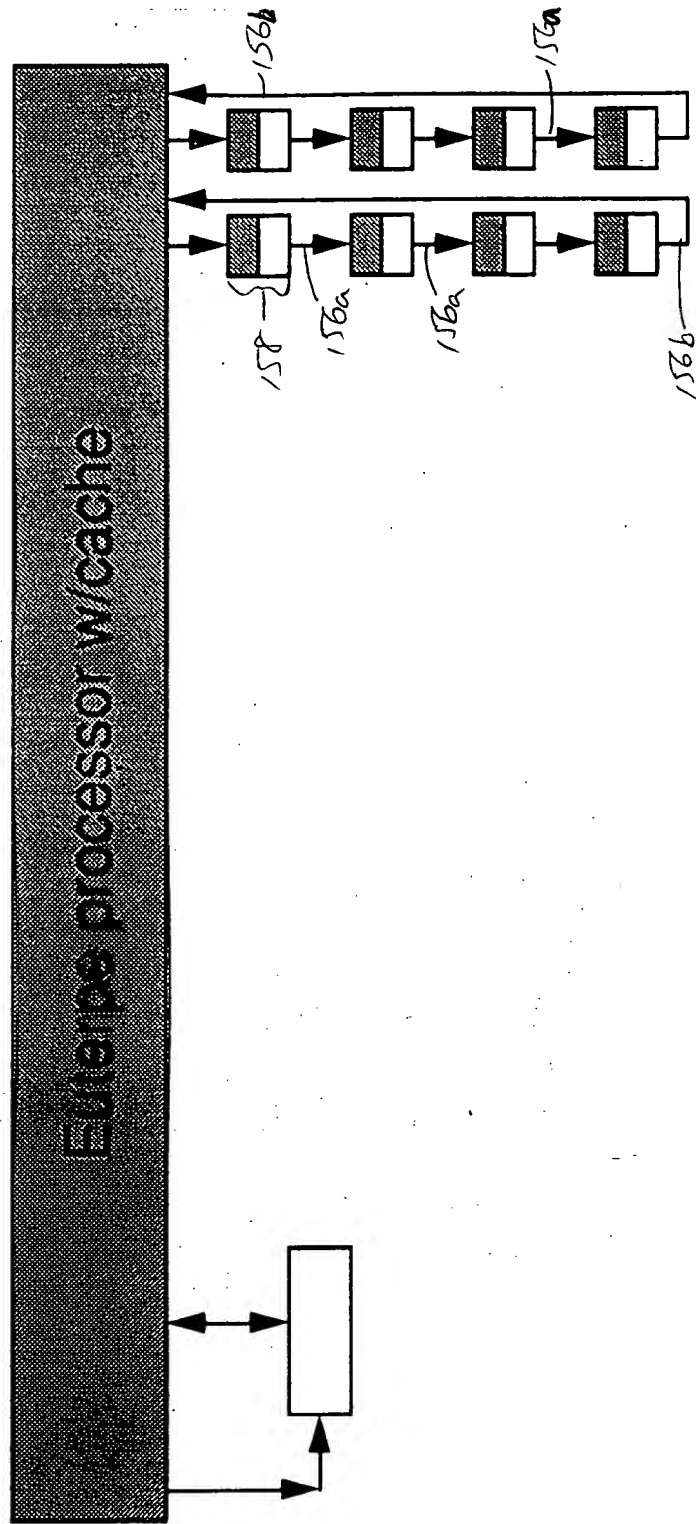


Figure 16(a)



The diagram illustrates a microprocessor system architecture. A central block labeled "Microprocessor w/cache" is connected to three main functional areas:

- 8 Memory channels (4 HiBRAM/ring):** This section consists of eight vertical channels. Each channel contains a stack of four HiBRAM/ring components. Bit widths are labeled as 2^{16} and 2^{10} .
- 9th ring for MP:** This section contains a single vertical channel with four components. Bit widths are labeled as 2^{16} , 2^{15} , and 2^{10} .
- 3 I/O channels:** This section consists of three vertical channels. Each channel contains a stack of four I/O components. Bit widths are labeled as 2^{16} , 2^{08} , 2^{08} , and 2^{16} .

Overall system bit widths are indicated by brackets on the right: 2^{16} for the memory channels, 2^{12} for the 9th ring, and 2^{14} for the I/O channels.

Figure 17

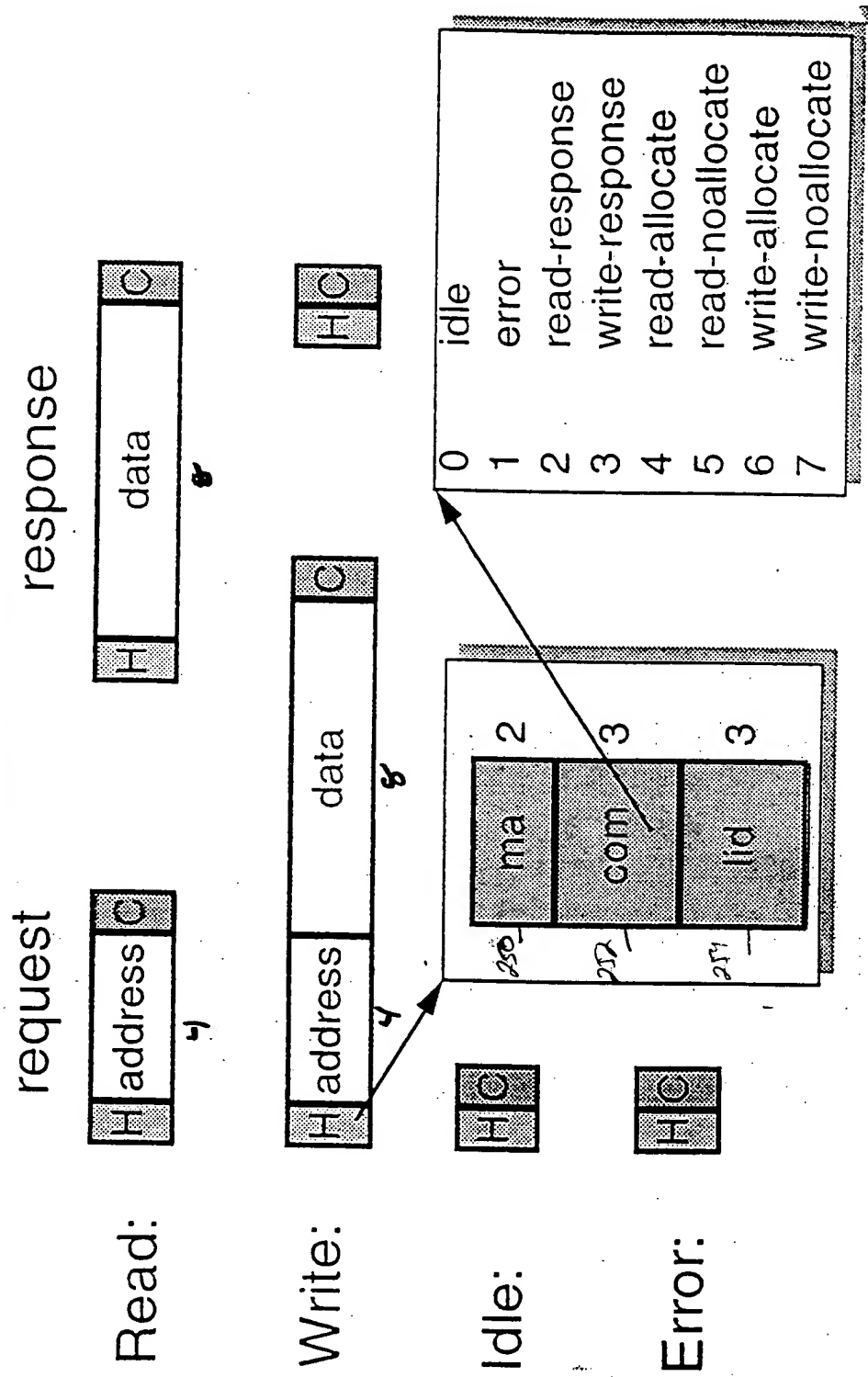


Figure 18

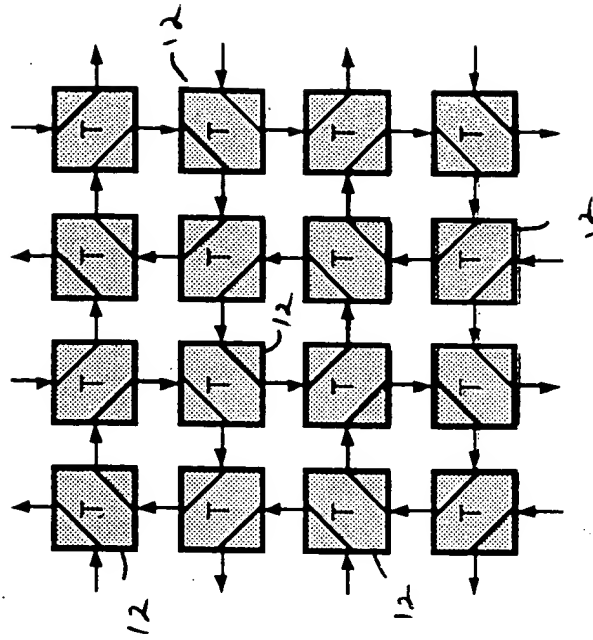
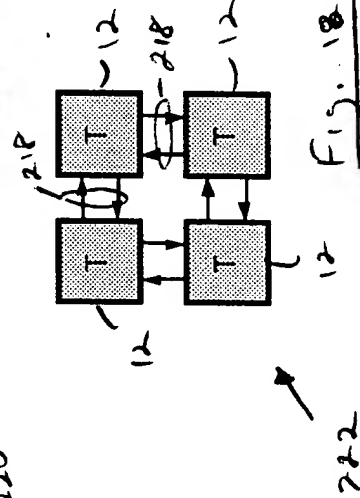
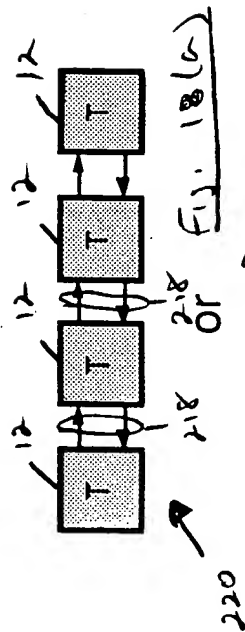
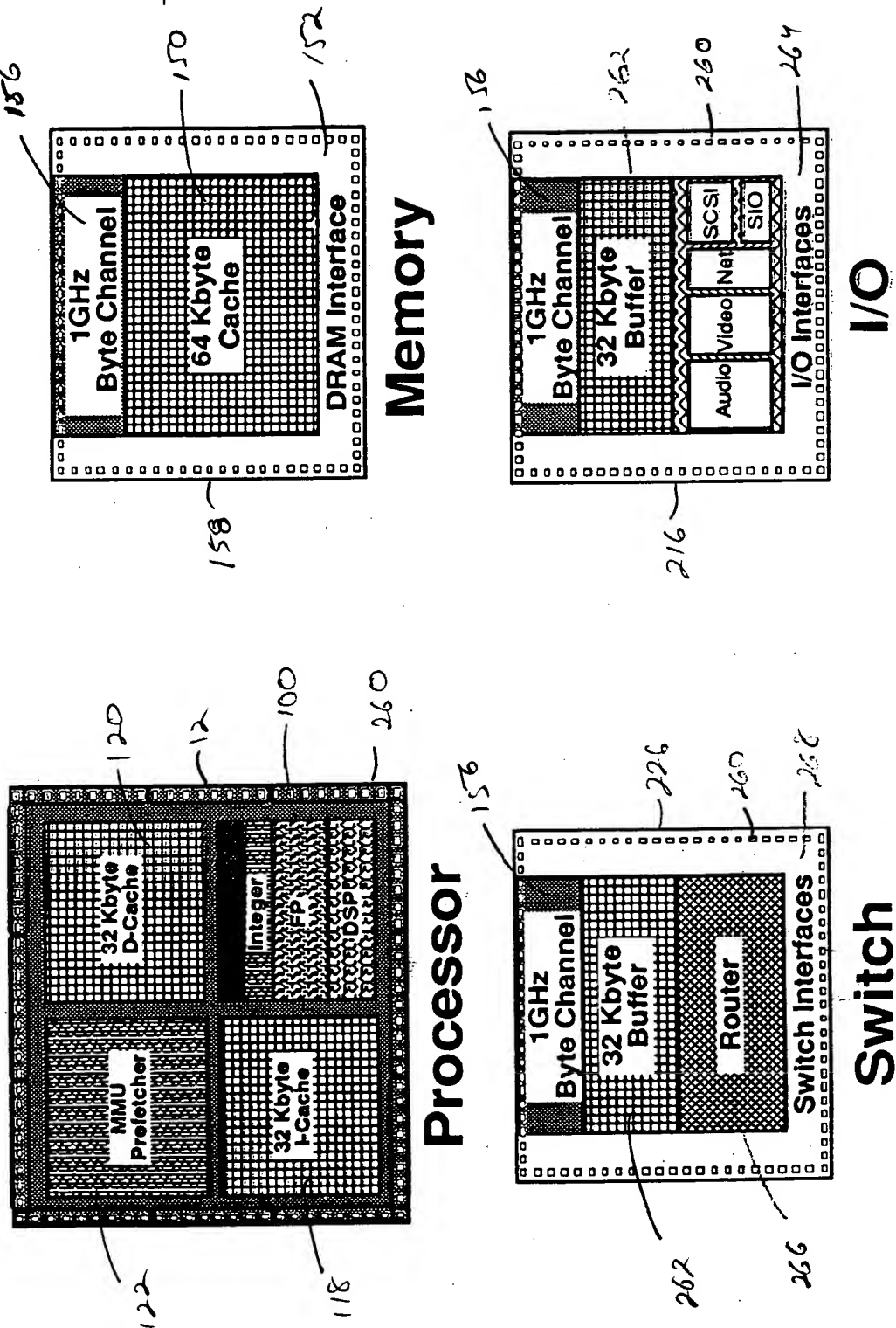


Fig. 18(c)

Figure 19



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